



The Low Power Programmable Leader

Lattice Competition

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Competitive Positioning – Where to win ?



**Lattice Avant™
Platform**



**Lattice Nexus™
Platform**



**Control & Security
FPGAs**



Lower Power



Smaller Size

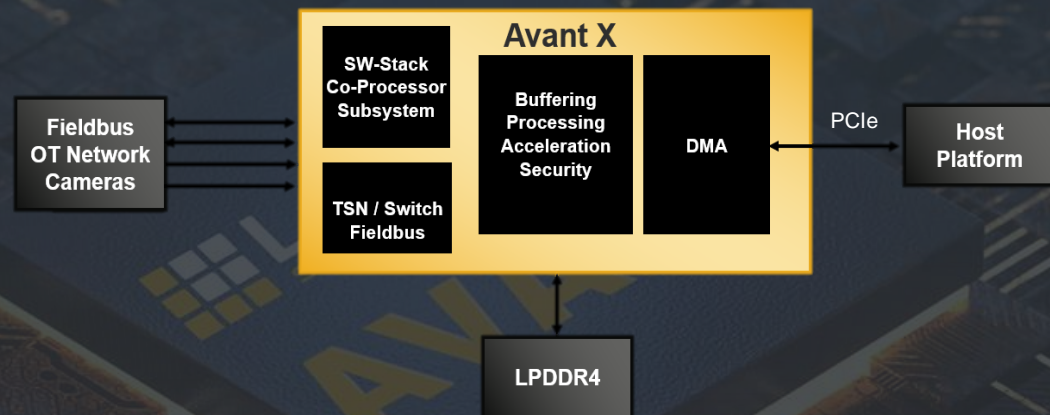


Faster Performance

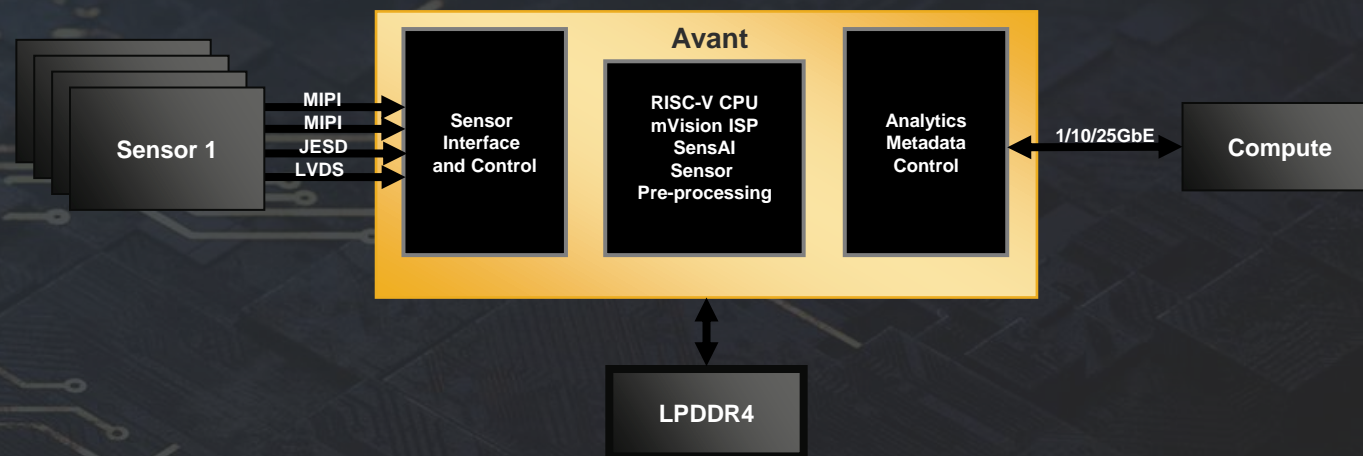
MID-RANGE FPGA PLATFORM LEADERSHIP

Lattice Avant™: Target Application Examples

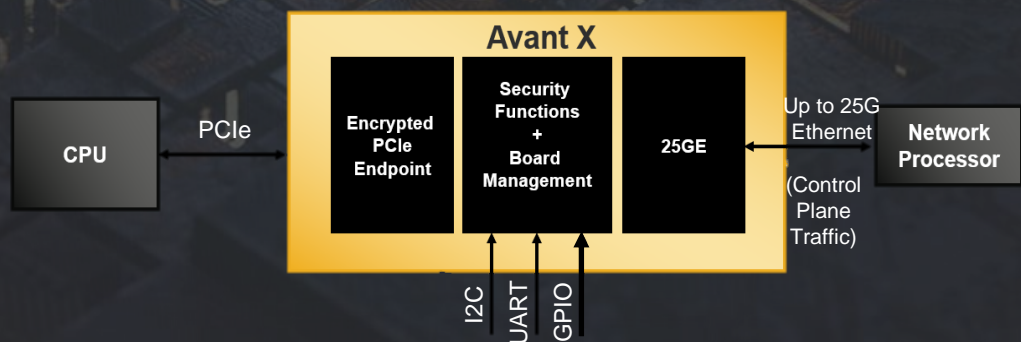
Industrial Networking NIC



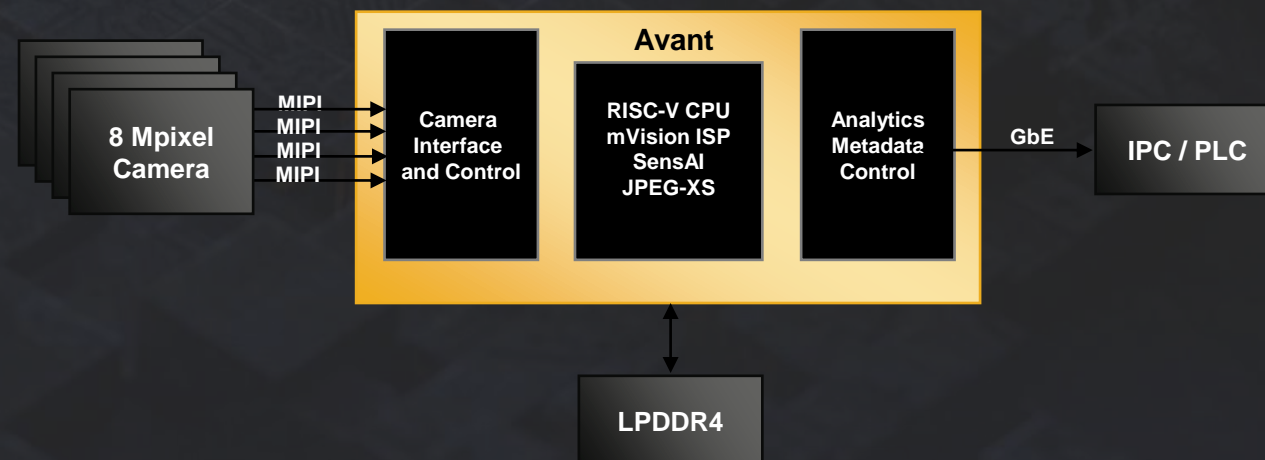
Sensor Streaming



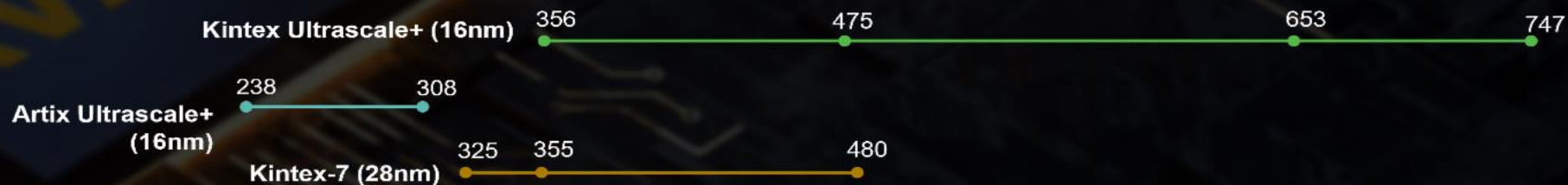
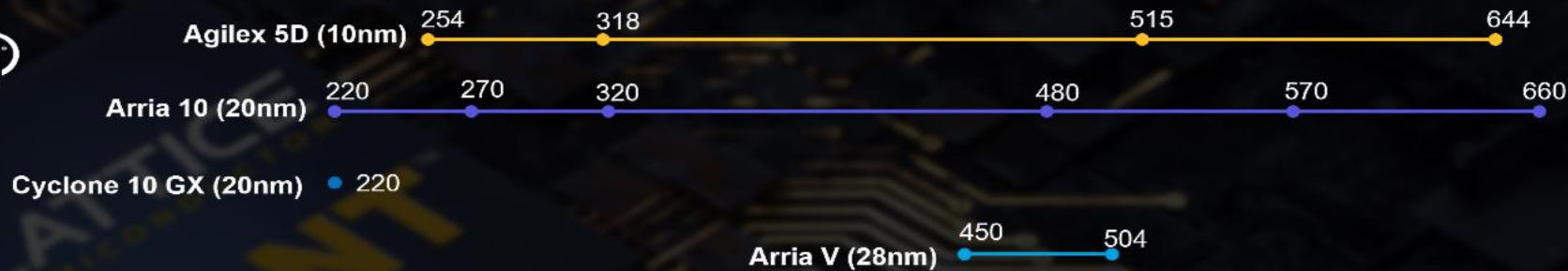
Packet Processing and PCIe Board Control



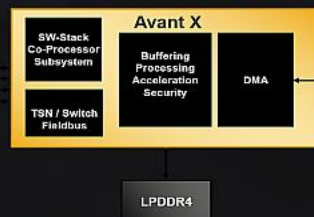
Machine Vision



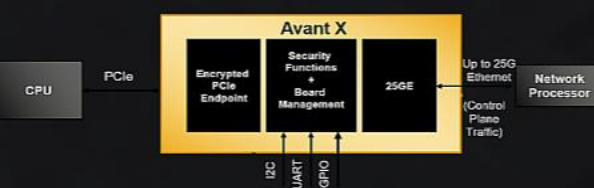
Avant Capacity Comparison



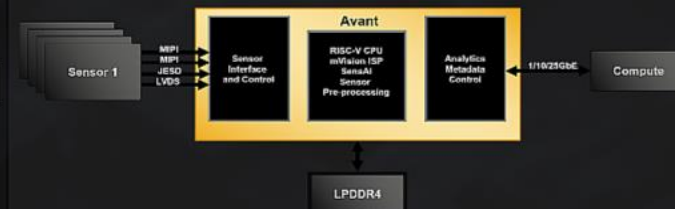
Industrial Networking NIC



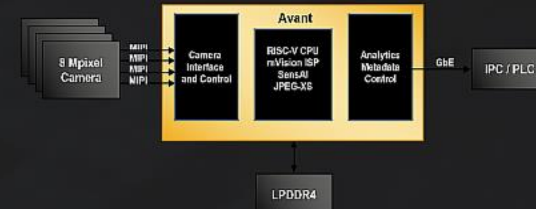
Packet Processing and PCIe Board Control



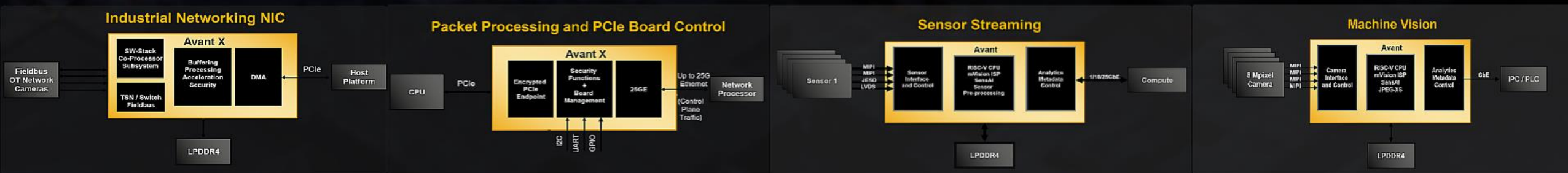
Sensor Streaming



Machine Vision



Lattice Avant Advantages





Lower Power



Fast Performance



High Reliability



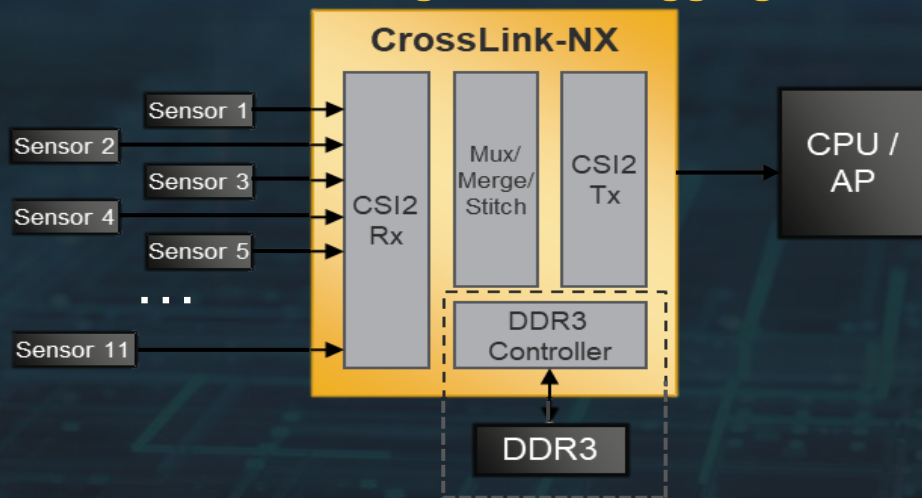
Smaller Size



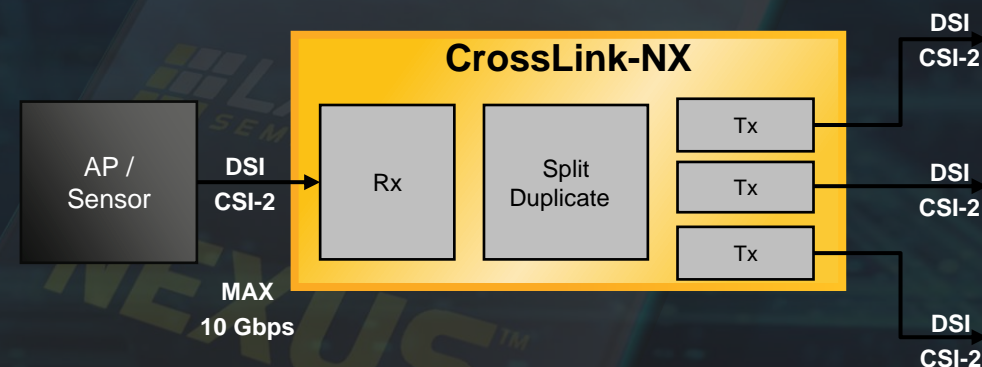
LEADERSHIP SMALL FPGA PLATFORM

Lattice Nexus™: Target Application Examples

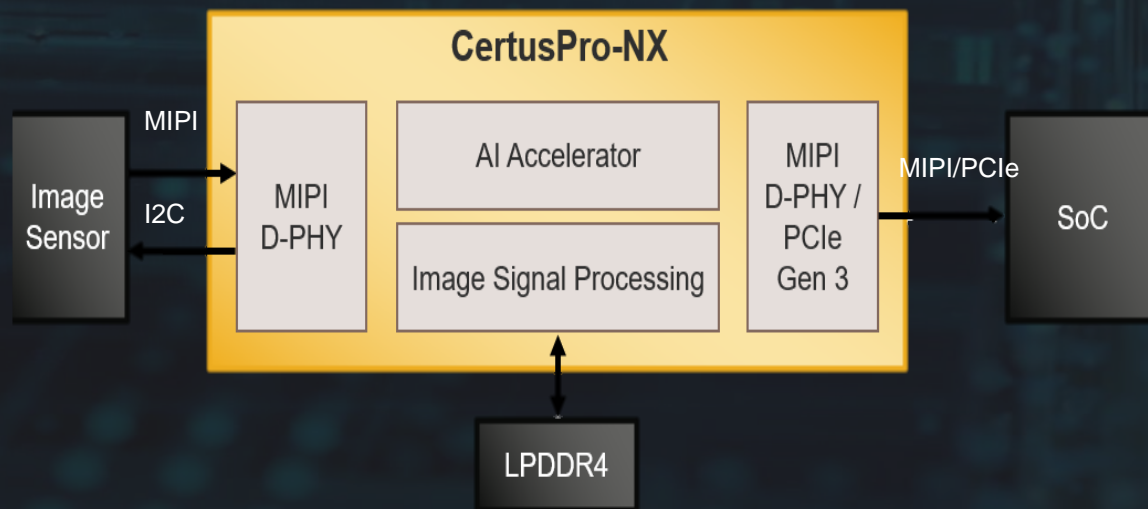
Multi CSI-2 Image Sensor Aggregation



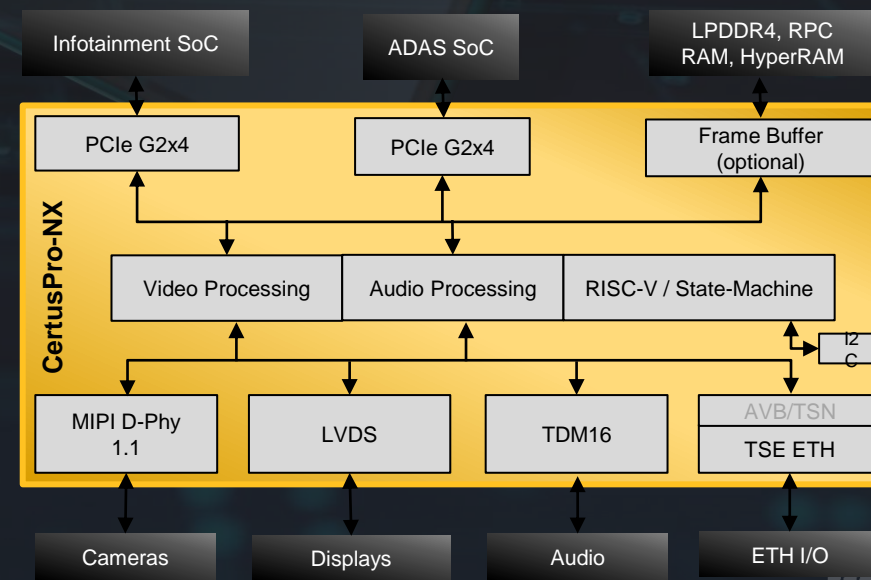
Display Splitting



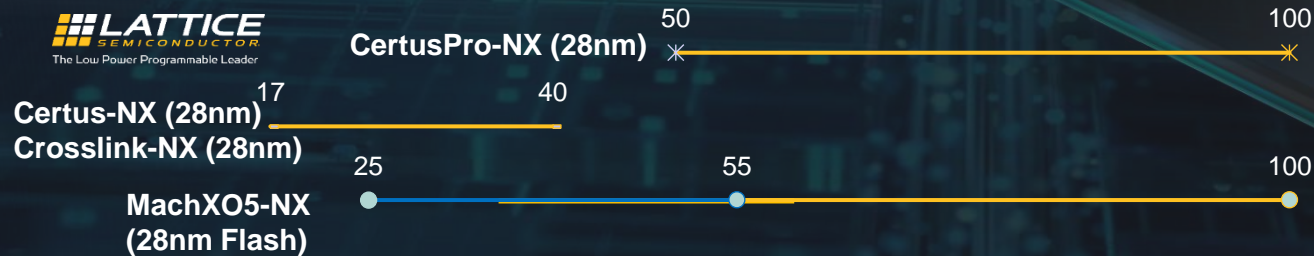
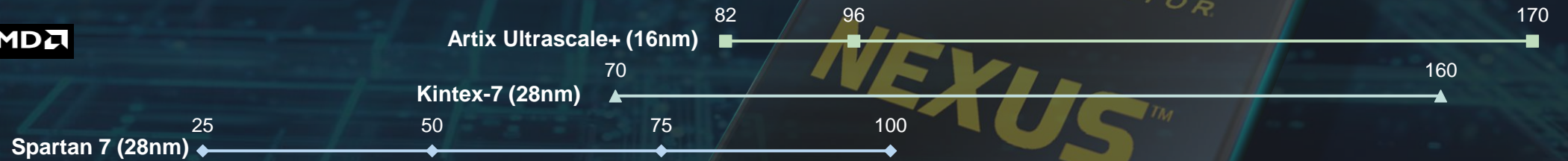
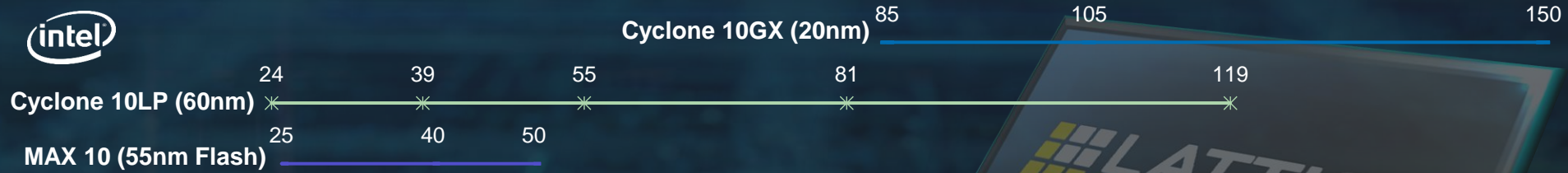
Smart Camera AI Processing



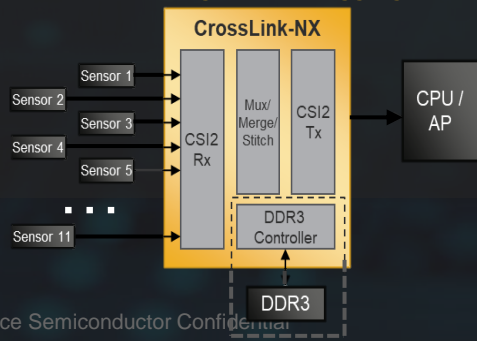
Interface Bridge (IVI/ADAS)



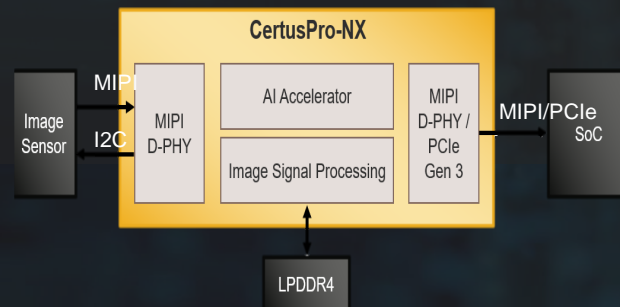
Nexus Capacity Comparison



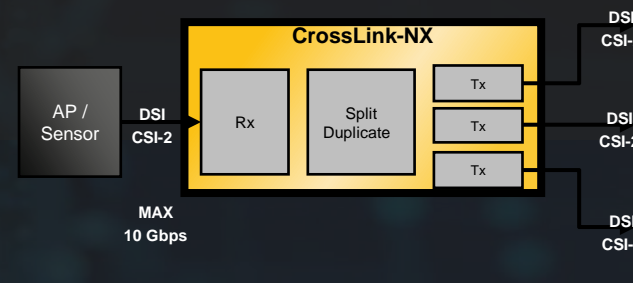
Multi CSI-2 Image Sensor Aggregation



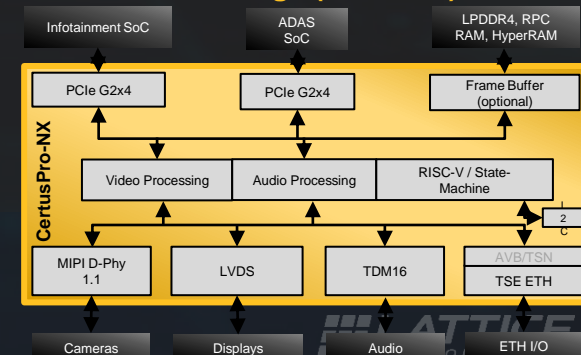
Smart Camera AI Processing



Display Splitting

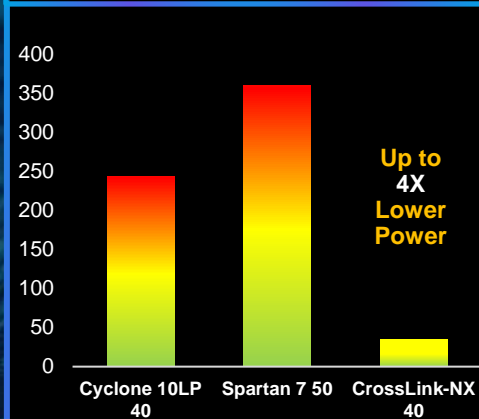


Interface Bridge (IVI/ADAS)



Lattice Nexus Advantages

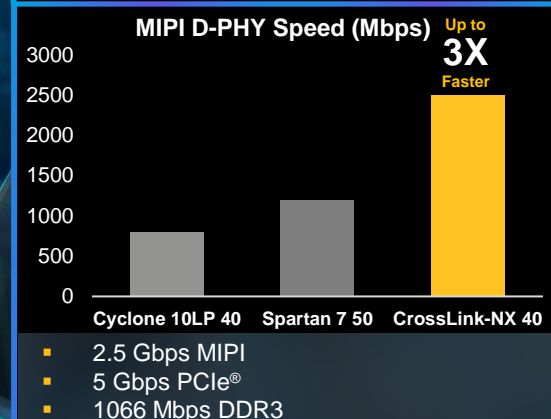
LOWER POWER



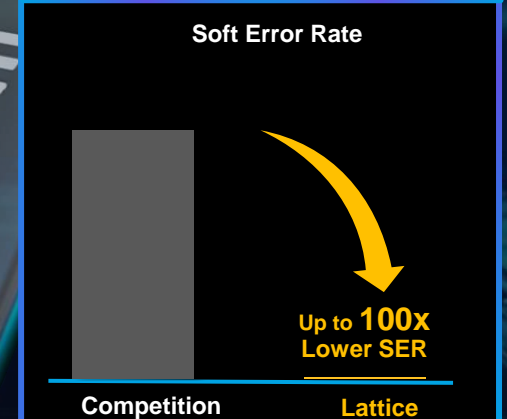
SMALLER SIZE



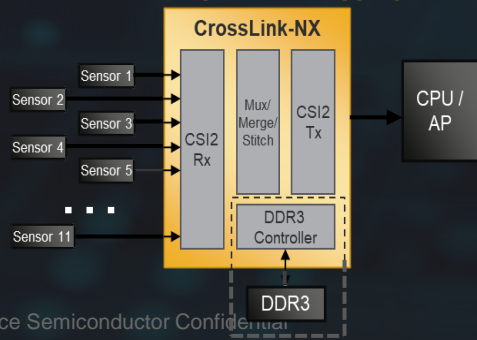
NEXUS D-PHY LEADERSHIP



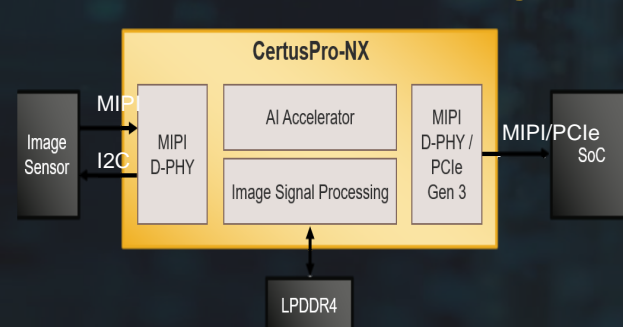
HIGH RELIABILITY



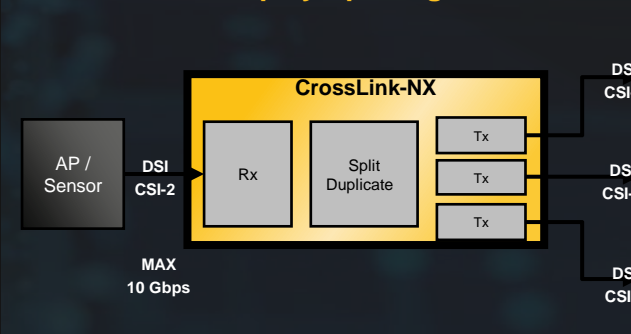
Multi CSI-2 Image Sensor Aggregation



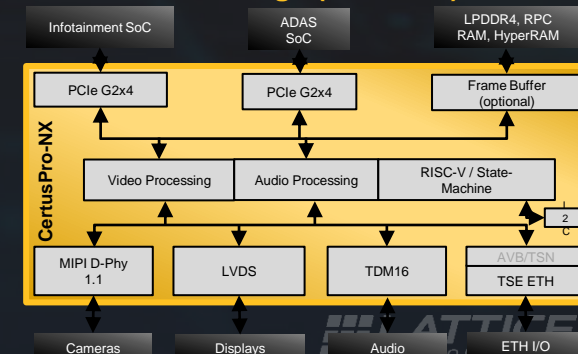
Smart Camera AI Processing



Display Splitting



Interface Bridge (IVI/ADAS)



COMPLIANT SECURITY FEATURES

- Hardware Root-of-Trust (RoT)
- Platform Firmware Resilience (PFR)
- Instant-on
- Integrated dual boot
- Post Quantum Cryptography (PQC)

FLEXIBLE I/Os & HIGH PROGRAMMABILITY

- High I/O count
- Various I/O voltage support
- Hot-socketing support

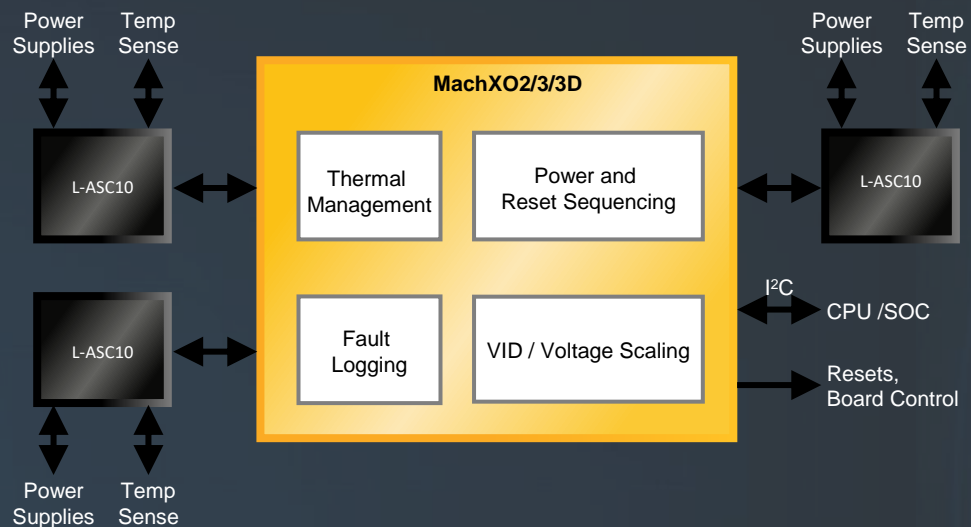
LOW POWER & SMALL FORM FACTOR

- Simplify thermal design
- Long lasting performance
- As small as 3 x 3mm in size

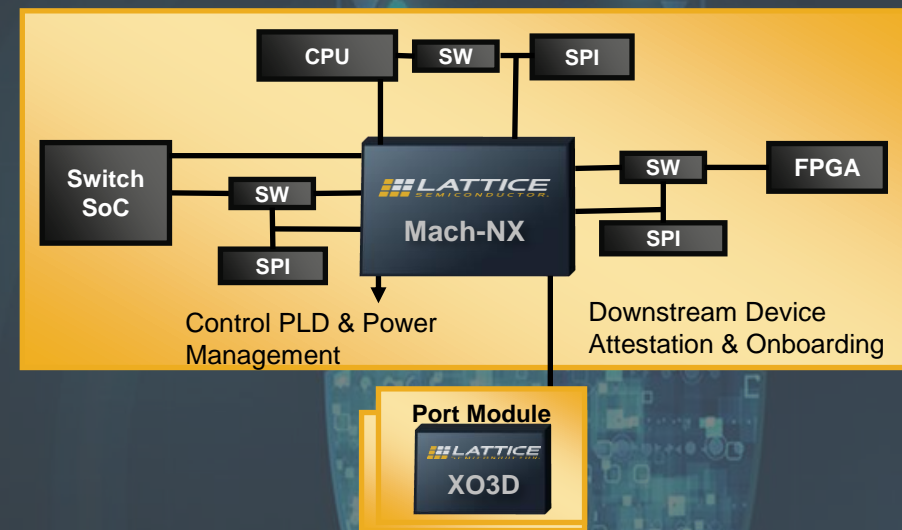


MachXO: Target Application Examples

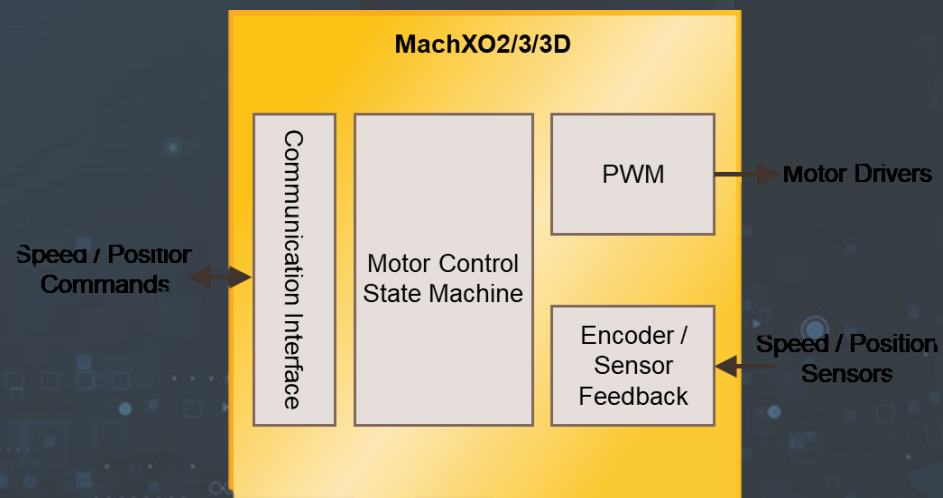
Hardware Management



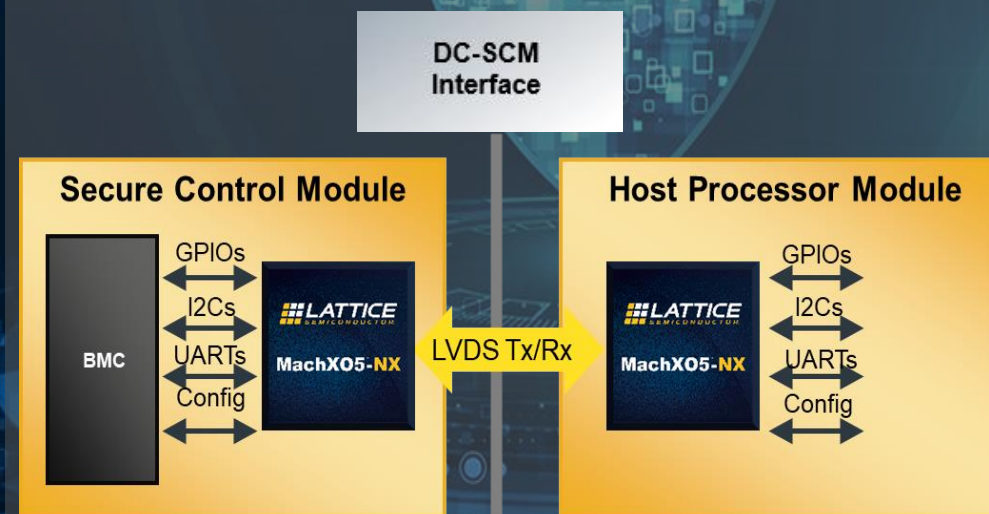
Network Switch



Motor Control



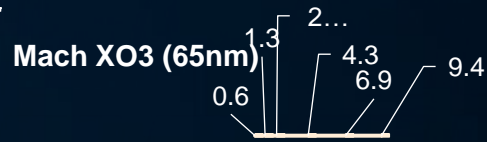
Secure Control Module



MachXO: Capacity Comparison



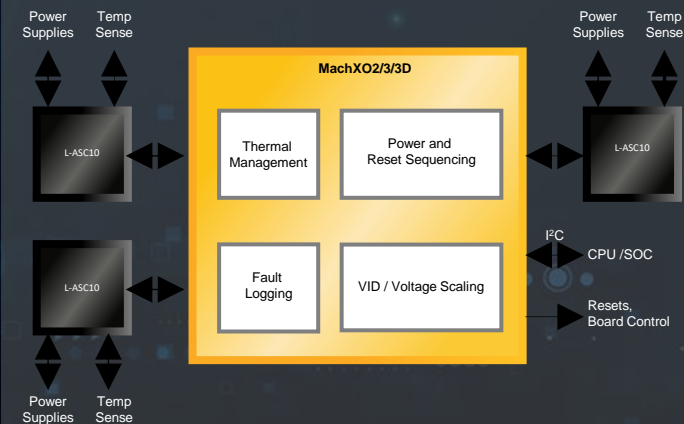
MAX 10 (55nm Flash)



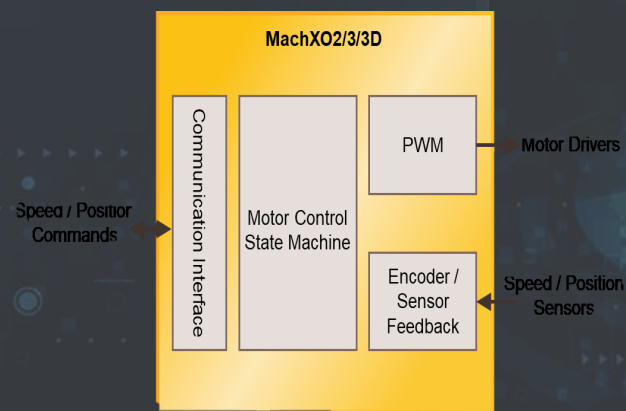
Mach XO2 (65nm)



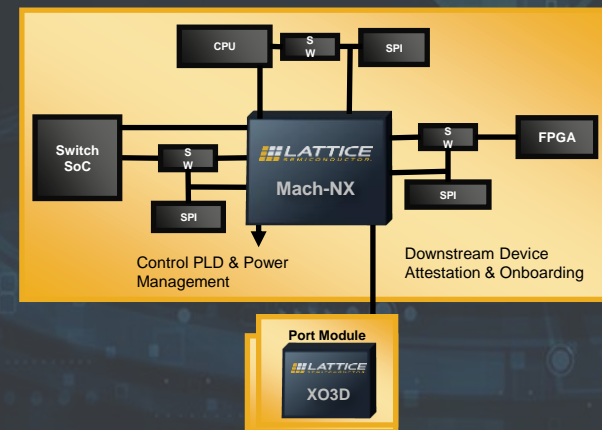
Hardware Management



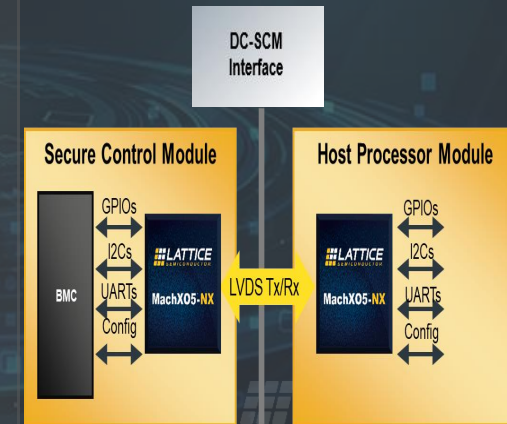
Motor Control



Network Switch



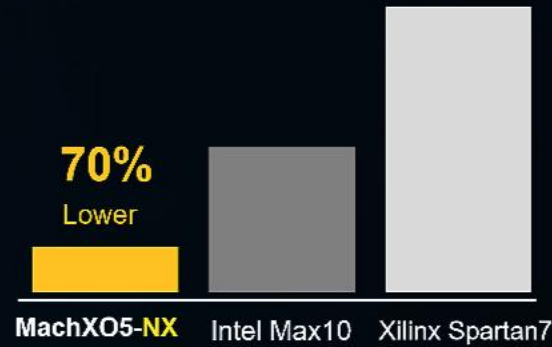
Secure Control Module



MACHXO Advantages

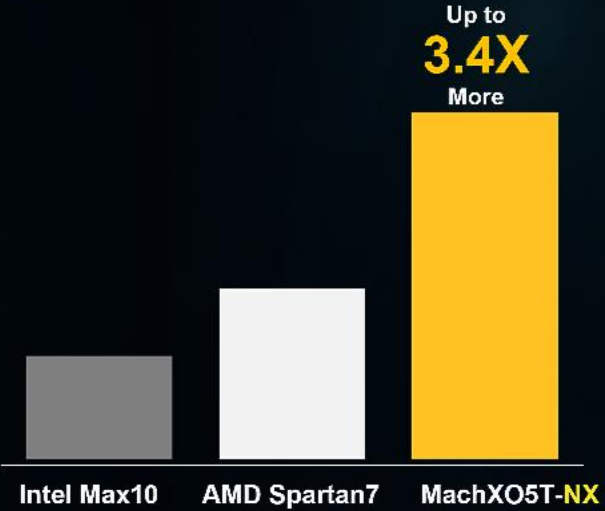
LOWER POWER

Static Power (worst case)*



EMBEDDED DEVICE MEMORY (kbit)

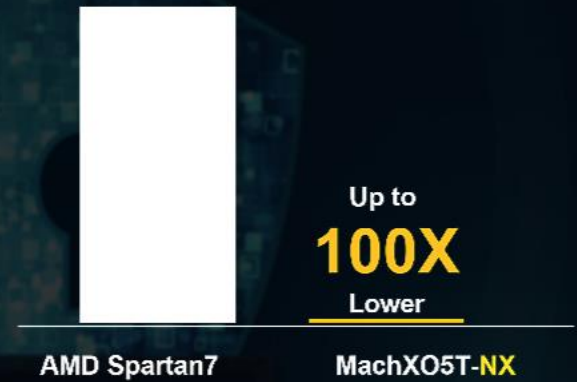
Reduces design footprint by minimizing the need for external memory



Comparable FPGA Density

SOFT ERROR RATE (FIT)

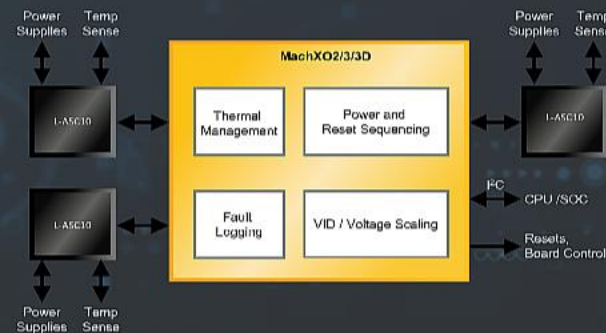
Lower soft error rate improves system reliability for safety-critical applications



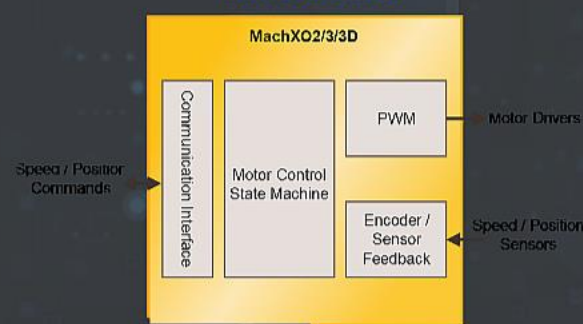
Intel does not publish SER performance data

LATTICE SEMICONDUCTOR

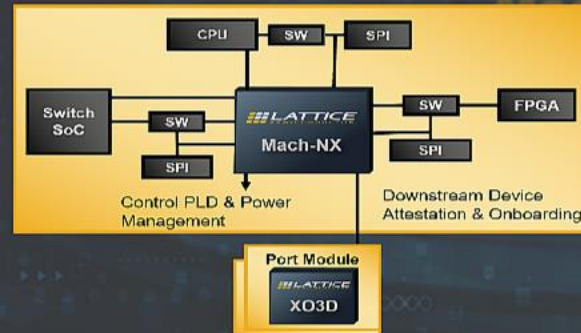
Hardware Management



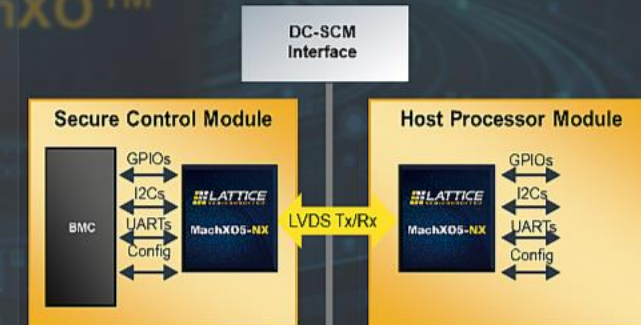
Motor Control



Network Switch



Secure Control Module



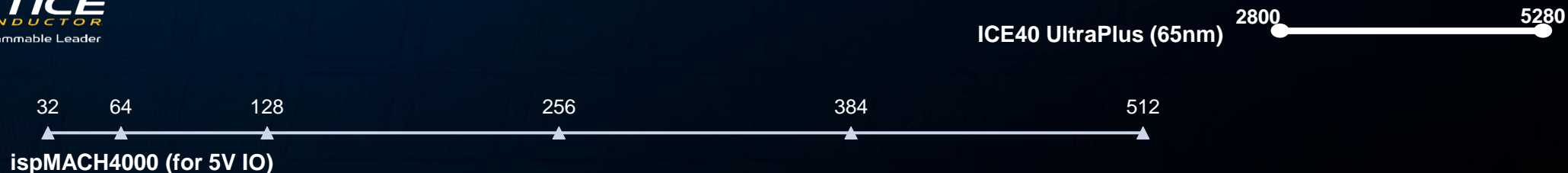
AMD End-of-Life Replacement

AMD EOL Replacement

- Product Change Notice XCN23009:

- CPLD

- CoolRunner CPLD (2002, 180nm) 32 to 512 macrocells
- XC9500XL CPLD (1998, 600nm) 36 to 288 macrocells



Lattice Alternative to XC9500 and CoolRunner-II CPLDs (macrocells)
Consider MachXO3 or ICE UP devices for non 5V tolerant IO designs

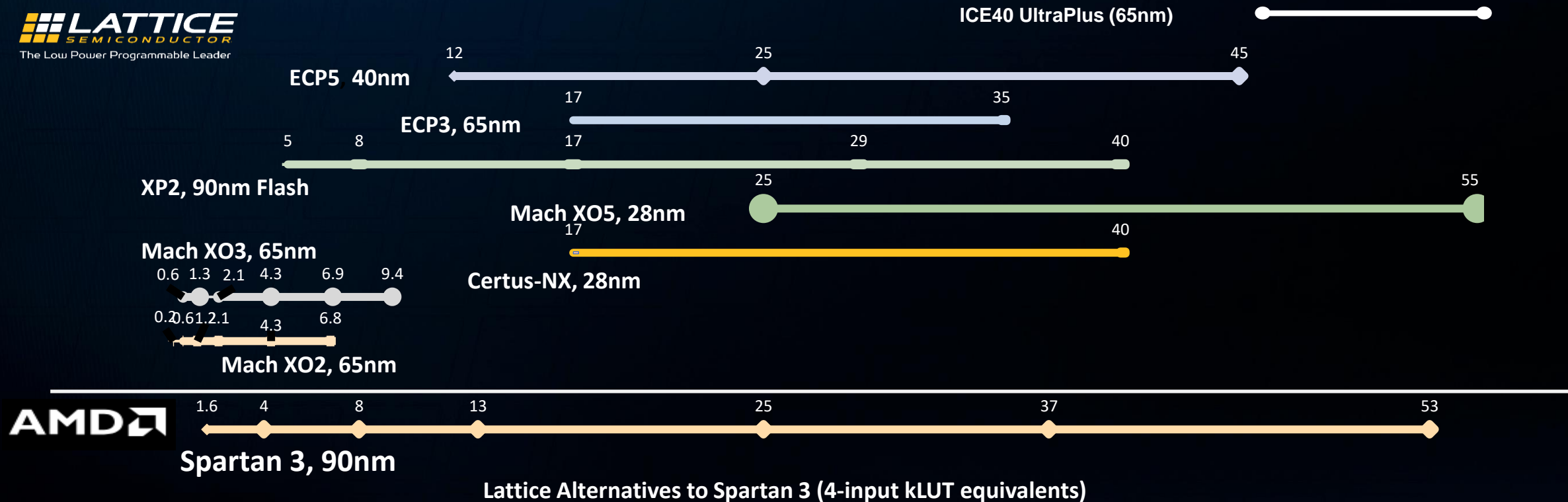


AMD EOL Replacement

- Product Change Notice XCN23009:

- FPGA:

- Spartan 3 FPGA (2003, 90nm) 1.5k to 50k Logic Cells
- Spartan 2 FPGA (1999, 150nm) 0.4k to 5.2k Logic Cells



More Resources Available

[Sales Resources](#) ✨

- Sales Toolbox – Presentations by marketing team for customers
- Channel Partners – Resources for Distribution Channel

[Lattice Insights On-demand Trainings](#) ✨

- Lattice Avant Platform Overview (19 Min)
- Video Connectivity Product Line Overview (21 Min)
- General Purpose Product Line Overview (54 Min)
- Control & Security Product Line Overview (1 Hr 13 Min)



[Lattice Avant Platform](#) ✨

- Demos
- White Papers

[Lattice Nexus Platform](#) ✨

- Introduction
- White Papers

[MachXO5-NX](#) ✨

- Reference Design
- Example Use Cases
- Documentation



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